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PTO/SB/33 (05-08)

PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 022150-000200US
<p>I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on <u>September 15, 2008</u>.</p> <p>Signature <u>Diane Hawley</u></p> <p>Typed or printed name <u>Diane Hawley</u></p>		Application Number 10/759,583 Filed January 15, 2004 First Named Inventor Kloth, Axel K. Art Unit 2624 Examiner Tsai, Tsung Yin
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p>		
<p>I am the</p> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>27.301</u></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____</p> <p><u>Kenneth R. Allen</u> Signature Kenneth R. Allen Typed or printed name (650) 326-2400 Telephone number September 15, 2008 Date</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p>		
<input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.		

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PATENT
Attorney Docket No.: 022150-000200US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Axel K. Kloth

Application No.: 10/759,583

Filed: January 15, 2004

For: METHOD AND APPARATUS FOR
IMAGE PROCESSING

Customer No.: 20350

Confirmation No. 8008

Examiner: TSAI, TSUNG YIN

Technology Center/Art Unit: 2624

ARGUMENTS IN SUPPORT OF
PRE-APPEAL BRIEF
REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicant, on behalf of the Real Party in Interest and assignee of the present invention, Parimics, Inc. a California corporation requests review and reversal of the Final Rejection dated May 15, 2008 of the above-identified application. This Request is filed with a Notice of Appeal after a Final Rejection, which is a second Final Rejection. A Response to the current Final Rejection has not been filed.

Status of Claims

Claims 1-17 stand finally rejected. System claim 1 and method claim 9 are independent, with claims 2-8 and 17 depending directly or indirectly on claim 1 and claims 10-16 depending directly or indirectly on claim 9.

Background for this Appeal

The Applicant has made a good faith effort to resolve all issues prior to appeal. This Appeal comes after two Final Rejections and a Request for Continuing Examination, a telephone conference interview with the Examiner and his supervisor in which the Inventor

participated, after the Applicant submitted the opinion of an expert, and after the Applicant attempted unsuccessfully to contact the Examiner after the Second Final Rejection.

The review of the Final Rejection is therefore requested for the reasons stated herein.

Rejection under 35 U.S.C. §103

The rejections are based on U.S. Patent No. 5,214,713 to Juvinal et al. ("Juvinal"), in view of U.S. Patent No. 5,535,288 to Chen et al. ("Chen") and further in view of U.S. Patent No. 5,708,209 to Shaw et al. ("Shaw").

Nature of the Invention

The claimed invention relates to a two-layer image processing system that has an image processing engine made up of parallel processors, one for each pixel, that in a first layer performs object-independent processing on a per-frame basis on data in integral registers of the engine and therefore without access to external memory. Further, it has a post processing engine formed of an N-way symmetric multi-processing system having N DFT engines and N matrix multiplication engines that performs object-dependent processing on the output of the image processing engine. Specifically, the system in its first layer is a massively parallel processor (MPP) that is of an systolic array type and configured as a single instruction multiple data (SIMD) system, wherein the image processing engine does not access external memory in its processing. The claimed method is the operation of the system. The Applicant submits that this is a new type of computer architecture.

Summary of Objections to Rejections

The Applicant has argued:

- +Juvinal neither processes image data one frame at a time nor retrieves and stores data in register integral with the image processing engine as required by claim 1. Neither Juvinal nor the other cited art of record discloses computational structures or processing on a per-frame basis without access to external memory.
- +Juvinal teaches away from claim 1 which recites in part processing engines that "directly receive ... data."
- +Chen does not teach or disclose an N-way Symmetric Multiprocessing (SMP) system having N DFT engines and N matrix multiplication engines. Chen in column 11, line 45ff very explicitly refers to an SIMD, which is definitely not an SMP.

+Shaw teaches only that instructions are held within pixel processors, similar to how instructions are held in an I-cache of any modern processor. There is no teaching or disclosure of image data being held within registers of a plurality of pixel processors, as recited by present claim 1.

The arguments advanced by the Applicant were also substantiated by Dr. John Gustafson, a well-recognized expert in the area of parallel and distributed computing (cf CV posted at the government site www.scl.ameslab.gov/Personnel/john.html and more currently at www.johngustafson.net, where it will be noted among other things that he has been on the editorial board of *Journal of Parallel and Distributed Processing* for more than ten years). The Examiner rejected all of Dr. Gustafson's findings and challenged his credentials as if they were part of the arguments in support of the claims. Most egregiously, the Examiner in the second Final Office Action of May 15, 2008, in paragraph 15, responded that it would have been "obvious to one skill(sic) in the art to employ Chen teachings to Juvinall to clarify the design of the post-processing engine and combine with Shaw to avoid memory bandwidth restrictions," when the expert Dr. Gustafson had explicitly declared that Juvinall, Chen and Shaw do not stand for the propositions advanced by the Examiner.

Observations on Examiner's Rejections

The Applicant submits that the Examiner has failed to obtain a thorough understanding of the invention disclosed and claimed in the application under examination by evidently failing to read and understand the specification, including the claims, as required by Examination procedures (MPEP 2100).

The Applicant submits that Examiner has applied the standard of obviousness improperly by misinterpretation of the relevance of the Juvinall reference to the claimed invention, especially as amended, in combination with other references.

The Applicant submits that the Examiner has misconstrued the Juvinall reference to apply to structures recited in the currently pending claims as amended, when in fact Juvinall discloses no such structures.

As a first example of misconception, the Examiner has posited his own definition of "object-independent processing," disregarding the explicit definition set forth in paragraph 22, lines 13-14 of the Applicant's Specification, where "object-independent processing" is defined as "processing of pixel data that have not been associated with any

objects." Disregarding the explicit definition provided by Applicant, the Examiner, in the Office Actions of 7/19/2007, of 10/23/2007, of 5/15/2008, has asserted that Juvinal teaches object-independent processing because he "discloses that object of interest for processing is that of the bottle-cap, which is seen independent of the bottle for processing." Clearly, "selecting an object of interest for processing" is completely contrary to the definition of "object-independent processing!" By this re-definition, the Examiner misconstrues the Juvinal reference to apply to structures recited in the currently pending claims.

As a further example of misconstruction and failure to understand both the disclosed invention and the cited art, the Examiner has asserted that Figure 6 of Juvinal discloses the integral registers of claim 1. This is clearly wrong. The claimed registers are integral to the systolic array processors (object-independent layer), while the registers in Juvinal's Figure 6 are 64-bit registers "associated" with the discrete microprocessors that constitute Juvinal's data-dependent processing layer. These registers are interposed between main memory and the microprocessors and serve to minimize the number of memory accesses required to fetch data that has been processed by Juvinal's systolic processor array. Again, the Examiner has misconstrued elements of the Juvinal reference in order to apply Juvinal to structures recited in the currently pending claims.

In a further example of failure to understand the disclosed invention and the cited art, the Examiner has asserted that Juvinal in Figure 2 discloses processing being performed on a per-frame basis. However, as pointed out by the Applicant, Juvinal describes extracting only two columns of pixels per frame. Juvinal then teaches that image process does not begin until two different and complete views of the imaged object have been acquired. Creating two complete views requires storing in a host memory these two columns from each frame of all the frames taken at equal intervals of rotation during one complete rotation of the object being imaged. In a given example, Juvinal teaches that up to 360 frames of data must be acquired before image processing can begin.

The Examiner appears to have extracted conclusions out of thin air from the Juvinal reference. For example, the Examiner has asserted that the art supports the claimed combinations of an internal register-oriented SIMD and a SMP. The invention is a combination of an MPP SIMD and an SMP-type DFT/Matrix Multiplication engine. Yet nowhere in the art of record are there such structures shown or suggested in the claimed combination.

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notwithstanding the Examiner's citation of individual components. At the time such prior art came into existence, the technology did not exist to make this combination.

The Examiner does not appear to be able to articulate his rejections in clear and proper language. His written expression in the English language is frequently grammatically incorrect and thus difficult to understand. His logic is flawed and full of non-sequiturs, which makes reasoned responses doubly difficult.

With all due respect, in nearly thirty-five years of practice, the undersigned attorney has never encountered the dismissal of the opinion and disparagement of the credibility of an expert by a Patent Office Examiner.

CONCLUSION

If the Examiner wishes to withdraw his Final Rejection and consider more fully the arguments previously made or to suggest amendments consistent with the scope of distinctions of the invention over the art, the Applicant would invite the Examiner to call the undersigned at the number given below. However, in view of prior amendments and proofs of record, the Applicants respectfully request reversal of the Final Rejection and issuance of a formal Notice of Allowance.

Respectfully submitted,



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